EE/CprE/Se 491 Weekly Report 3
9/26/24 - 10/3/24
sdmay25-28
Digital ASIC fabrication
Client & Advisor: Dr. Duwe

Team Members

Calvin Smith – Issue Tracking/Toolchain Figure-outter
Camden Fergen - Testing Lead
John - Team organizer
Nicholas - Verilog Lead
Levi - Client interaction

Weekly Summary

This week we focused on setting out a future roadmap that we can use to guide us and allow us to get a good overview of what we are to expect. Creating the future roadmap will help us make sure that we have a good plan and see what Dr. Duwe thinks about our plans. It will also help us make sure we do not run into any roadblocks that were not expected. Unexpectedly, we have pivoted our direction from either BMSIC/EInk to Custom ISA due to feedback from Dr. Duwe, this will hopefully be our final direction of pursuit going forward.

Pask Week Accomplishments

- Calvin:
    - Pivoted from verilog floating point design due to drastic changes brought by our advisor meeting
    - Explored options regarding existing RISCV chips we can use for extension
    - Found a likely customizable chip repository
    - Installed rocket-chip and it's dependencies on top of getting chisel to work on a local machine for transpiling scala to verilog
    - Began tutorial work for chip fab software and installed requisite caravel project files
    - Did the advisor meeting summary part of this report
- Camden:
    - Created project planning spreadsheet to ensure team stays on track during the project
    - Helped team to ensure we got our weekly assigned homework completed in time and also well done

    - Lead planning meeting with team
- John:
    - Researched FPGA fabrics
    - Familiarize myself with Caravel
    - Future project planning
        - Tentative roadmap
    - Familiarized myself with RISC-V
- Levi:
    - Researched RISC-v instruction set
    - Installed rocket-chip and it's dependencies on top of getting chisel to work on a local machine for transpiling scala to verilog
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- Nicholas:
    - Did research on RISC-V instruction set.
    - Did research on FPGA design
        - Did preliminary designs to see the feasibility of an FPGA.
    - Started working with Open Memory to add memory for datapath 2 of CprE 3810 Lab 2.
    - Hardened Design of datapath 1 in project wrapper.

Name	Individual Contribution	Hours this Week	Hours Cumulative
Calvin	Tested and decided on RISCV implementation for use with our project Explored potential toolchains for use with verilog	6.3900	18.2532
Camden	• Created project planning sheet to track progress of project • Lead team planning meeting	6	18
John	• Researched FPGA fabrics • Worked on tentative roadmap • FPGA Research	6	18
Levi	• Worked on roadmap • Caravel research	6	18
Nicholas	FPA and RISC-V research	6	20

	Worked on implementing Lab2 datapath.		

Plans for Upcoming Week

- Calvin:
  - Continue work with getting the rocket-chip toolchain up and running, hopefully getting a default config from the rocket-chip repo compiled to verilog, hardened, and visualized
  - Complete at least the first tutorial regarding the Chipfab/Efabless toolchain
- Camden:
  - Continue work on team planning doc to encompass and be more specific on tasks
  - Work with team members and work through getting lab 1 and 2 from CprE 381 hardened
- John:
  - Dedicate time into caravel and Efabless
  - Generate datapath for CPRE 3810 lab 2
  - Research more about Caravel
- Levi:
  - Harden datapath of CPRE 3810 lab 2
  - Learn to compile scala to verilog and hardening using rocket-chip
  - Create limitations and guidelines for our project interacting with Caravel
- Nicholas:
  - Get datapath 2 hardened with the project wrapper.
  - Start working on verilog files for FPGA/Processor

Summary of weekly advisor meeting

After presenting both of our ideas that we had narrowed down to Dr. Duwe, we had both shot down and was told that he liked one of our previous ideas, being the Custom/Programmable ISA implementation better. After this was clear, we discussed some of the potential problems regarding the idea, involving the tradeoffs between conversion of our 381 MIPS CPU to RISCV versus trying to use an open-source preexisting RISCV implementation we could extend. Due to the fact we would be flying in the dark when it comes to the conversion of our MIPS CPU because the testing resources are MIPS based, we ended up deciding to source a RISCV implementation from somewhere else (likely UC Berkeley's rocket cores, although this is still up for some debate).